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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Case No. 5:17-cv-05671-BLF-NC **FILED UNDER SEAL** **PLAINTIFF VLSI TECHNOLOGY LLC'S RESPONSE TO DEFENDANT INTEL CORPORATION'S OMNIBUS MOTION FOR SUMMARY JUDGMENT** Date: October 19, 2023 Time: 9:00 a.m. Courtroom: 3 (5th Floor) Judge: Hon. Beth Labson Freeman

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Intel Corporation's ("Intel") Motion for Summary Judgment ("Mot.") presents a litany of unsupported attorney assurances of "undisputed" issues, but those issues are subject to fundamental factual dispute. They also require the Court to disregard the parties' stipulations, dismiss its own claim constructions, rewrite patents, and contradict another court's prior rulings on the same issues. VLSI Technology LLC ("VLSI") respectfully requests that the Court deny Intel's omnibus motion.

I. LEGAL STANDARD

Summary judgment is appropriate only if "there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law," and when "no 'reasonable jury could return a verdict for the nonmoving party.'" *Spigen Korea Co. v. Ultraproof, Inc.*, 955 F.3d 1379, 1383 (Fed. Cir. 2020) (quoting *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986)).

II. INTEL INFRINGES THE '836 PATENT

A. Background

***'836 Patent*:** Microprocessors are often referred to as the "brain" of a computer system. Some modern processors—called multicore processors—include multiple sets of circuitry called "cores." Each core can execute computer instructions. Multicore processors are advantageous in that they can execute instructions in parallel. Each set of instructions that a core executes is called a thread. A processing task (e.g., an application) can have one or more active threads. Some processing tasks, for example, may only have one active thread and thus can only be run on a single core, whereas other processing tasks can be run across multiple cores simultaneously.

The '836 Patent relates to particular architectures and methods of operation of multicore processors that substantially improve processor performance. The inventors recognized that different cores—even those intended to be identical—can operate at higher or lower frequencies at a given voltage due to manufacturing variations. They appreciated that those performance differences can be measured and recorded, and that such information can in turn be used to optimize system performance by directing single-core processing tasks to the fastest core(s) based on their recorded performance characteristics. *See, e.g.*, ECF 1-8 ('836 Pat.) at 1:7–20; 1:56–67; 2:5–13; 9:65–10:3. By taking advantage of stored maximum per-core frequency information, "a job that cannot be run across multiple cores [can be run] in the fastest core, thereby improving the device

performance . . . without substantially increasing the power. In this way, jobs that cannot be distributed across multiple cores can now be executed on a single core which can run at a higher frequency than the nominal frequency at the nominal voltage." *Id*. at 2:7–13.

[redacted]

B. Intel Is Not Entitled To Summary Judgement Of No Literal Infringement

VLSI's expert Dr. Thomas Conte explains how Intel's Accused Products literally infringe claims 1, 9–11, 13, 17, 20, and 21 of the '836 Patent. *Id.* ¶¶ 300–600. At issue here is representative step 1[d], which recites: "upon identifying a processing task that cannot be run across the plurality of cores, selecting a core from the plurality of cores having a fastest measured processing speed parameter at a given voltage to run the processing task." ECF 1-8 ('836 Pat.) at 10:50–54.

[redacted]

[redacted]

Intel's motion for summary judgment of no literal infringement is premised on a mischaracterization of Dr. Conte's infringement opinion. [redacted]

[redacted]

C. Intel Is Not Entitled To Summary Judgement Of No Infringement Under DOE

[redacted]

[redacted]

[redacted]

1. Amendment-Based Estoppel Does Not Apply

It is undisputed that claims 1 and 10 have always included the "upon identifying" claim language and were not narrowed during prosecution. Ex. 10 ('836 File History) at 1824–25; Mot. at 5. Claims 1 and 10 were rejected based on Bernstein and Kim, Ex. 10 at 1849, -86, while claim 20 was rejected based on Bernstein and Ghiasi, *id*. at 1856, -93. Claim 20 had an additional limitation not present in claims 1 and 10. *Id*. at 1941 ("running a multi-core application on a plurality of the multiple cores . . ."). In response to the Applicant's arguments, *see id*. at 1877–79 (7/25/12 Resp.); *id.* at 1904–06 (12/28/12 Resp.); *id.* at 1913–1916 (3/12/13 Br.), the Examiner *withdrew* the rejection of all claims, *id*. at 1928. The Examiner then initiated a further interview and proposed two "clarifying" amendments: (1) in claims 1 and 10, "replacing "by" with "across" and adding "at a given [specified] voltage"; and (2) adding "upon identifying a processing task that cannot be run ***across*** the plurality of multiple cores" to claim 20, for allowance. *Id*. at 1934, 1936, 1938–41.

The Applicant's agreement to amend claim 20 does not trigger prosecution history estoppel because the clarifying amendment was not made to overcome the prior art. *Intendis GmbH v. Glenmark Pharms. Inc.,* 822 F.3d 1355, 1365–66 (Fed. Cir. 2016) (amendment-based estoppel did not apply where there was a "clarifying amendment" rather than a "narrowing amendment"). First, there was no pending rejection of the claims. Ex. 10 ('836 File History) at 1928 (Examiner withdrawing rejections). Second, the Bernstein and Kim references discussed during the interview did not relate to claim 20 because the Examiner relied on a different obviousness combination (Bernstein and Ghiasi) for claim 20. *Id*. at 1934. Finally, the addition of the "upon identifying" to claim 20 "did nothing more than make express what had been implicit in the claim as originally worded," as this language had been present in claims 1 and 10 from the beginning. *Interactive Pictures Corp. v. Infinite Pictures, Inc.*, 274 F.3d 1371, 1377 (Fed. Cir. 2001). *Old Town Canoe Co. v. Confluence Holdings Corp.*, 448 F.3d 1309 (Fed. Cir. 2006), is distinguishable because, unlike here, the claim in question was amended "in response [to] a rejection by the examiner to include the limitation that coalescence comes to completion," *id.* at 1314–15.

Even if the amendment had been narrowed (it was not), the presumption of surrender of all equivalents can be overcome by showing that the amendment "[bore] no more than a tangential relation to the equivalent in question." *Eli Lilly & Co. v. Hospira, Inc.*, 933 F.3d 1320, 1330 (Fed. Cir. 2019). That is especially the case here. The amendment to claim 20 does not trigger prosecution history estoppel because the order or timing of events (upon identifying before selecting) had nothing to do with the Examiner's initial rejection of the claims. The issue was whether the prior art disclosed the "identifying" limitation at all. Ex. 10 ('836 File History) at 1877–79, 1904–06, 1913–1916. Nor does the Examiner's Interview Summary suggest a timing requirement. The focus of the Examiner's statement that "[i]t was agreed to amend independent claims 1, 10, and 20 to clarify that a core is selected from the plurality of cores when it is identified that a task cannot be run ***across*** the plurality to of cores," *id*. at 1934, was to change the word "by" to "across" as reflected by amendments to claims 1 and 10. It had nothing to do with timing. Indeed, "when" was not added to the claims. Therefore, the Applicant's amendment to claim 20 is at most a tangential change unrelated to the timing of selecting a core "upon identifying a single core task." *See Eli Lilly*, 933 F.3d at 1331 ("We therefore hold that Lilly's amendment was merely tangential to pemetrexed ditromethamine because the prosecution history, in view of the '209 patent itself, strongly indicates that the reason for the amendment was not to cede other, functionally identical, pemetrexed salts."). As such, amendment-based estoppel does not bar DOE for the "upon identifying" limitation.

2. Argument-Based Estoppel Does Not Apply

Argument-based estoppel also does not bar VLSI's DOE theory. "To invoke argument-based estoppel, the prosecution history must evince a 'clear and unmistakable surrender of subject matter.'" *Deering Precision Instruments, L.L.C. v. Vector Distrib. Sys., Inc.*, 347 F.3d 1314, 1326 (Fed. Cir. 2003) (quoting *Eagle Comtronics, Inc. v. Arrow Commc'n Lab'ys, Inc.*, 305 F.3d 1303, 1316 (Fed.Cir.2002)). The clear and unmistakable standard is a high bar. *Silt Saver, Inc. v. Hastings*, 2017 WL 7053968, at *9 (N.D. Ga. Oct. 18, 2017); *AngioScore, Inc. v. TriReme Med., Inc.*, 50 F. Supp. 3d 1276, 1294 (N.D. Cal. 2014) (noting that "the application of the prosecution disclaimer doctrine" is cabined to "***unambiguous disavowals***" only.).

Although Intel invokes the Court's *Markman* order finding that the Applicant distinguished

claim 10 from the prior art on the basis of the "upon identifying" limitation, Mot. at 5 (citing ECF 241 (Order) at 24), that disclaimer, which was focused on whether claim 10 requires an "*identifying*" limitation at all, is inapplicable here. [redacted] inally, *Amgen, Inc. v. Coherus BioSciences, Inc.*, 931 F.3d 1154 (Fed. Cir. 2019), does not support Intel's position. *See* Mot. at 6. The *Amgen* Court held that argument-based estoppel applied because the applicant surrendered salt combinations other than those recited in the claims. *Amgen*, 931 F.3d at 1159–60. That is not the case here; no surrender of timing occurred.

3. Claim Vitiation Does Not Apply

Intel's claim vitiation argument should be rejected because it is based on a mischaracterization of VLSI's DOE theory. Intel incorrectly asserts, without citation, that under VLSI's equivalents theory, the claims are met "if a single-core task is sent to the fastest core for any reason, including those having nothing to do with whether the task is a single-core task." Mot. at 6. Not so. [redacted] This infringing mechanism delivers a performance benefit because a single-core task that is identified and run on the fastest core can be completed faster due to that core being run at a higher clock frequency. *Freedman Seating Co. v. American Seating Co.*, 420 F.3d 1350 (Fed. Cir. 2005), does not apply because VLSI's theory does not render "upon identifying" meaningless. *See* Mot. at 6.

Finally, Intel misapprehends the law on claim vitiation, which "is not an exception or

threshold determination that forecloses resort to the doctrine of equivalents, but is instead a legal conclusion of a ***lack of equivalence based on the evidence presented*** and the theory of equivalence asserted." *Bio-Rad Lab'ys, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1366–67 (Fed. Cir. 2020) (quoting *UCB, Inc. v. Watson Lab'ys, Inc.*, 927 F.3d 1272, 1283 (Fed. Cir. 2019)). A "holding that the doctrine of equivalents cannot be applied to an accused device because it 'vitiates' a claim limitation is ***nothing more than a conclusion that the evidence is such that no reasonable jury could conclude*** that an element of an accused device is equivalent to an element called for in the claim." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1018–19 (Fed. Cir. 2006). There is no basis for such a conclusion here.

D. Intel's Manufacturing Activities Meet The Limitations Of The Claims

Intel is not entitled to summary judgment of no infringement for method claims 1, 9, 20, and 21 based on territoriality. [redacted]

Intel is also not entitled to summary judgment of no infringement for apparatus claims 10–11, 13, and 17 because each Accused Product is "a multi-core system on chip" that includes "a performance measurement circuit for measuring a performance parameter value for said core." Ex. 1 (Conte Rpt.) ¶ 339 ("Each core includes performance measurement circuitry [that] . . . includes critical path monitoring circuitry for testing critical paths used for measuring such frequencies and voltages."). [redacted] d [redacted] 1. ECF 580-15 at 2.

III. INTEL INFRINGES THE '922 PATENT

Intel raises two arguments on summary judgment. [redacted]

First, the asserted claims do not forbid the claimed "supply signal" from being the "reference signal." To the contrary, the '922 claims expressly state when separately recited elements must read on separate features. *E.g.*, ECF 1-05 ('922 Pat.) cls. 1, 17 (requiring "second power characteristics" to be "[at least partially] ***different from***" "first power characteristics"), 9 (requiring one "switching threshold" to be at "a same switching threshold voltage" as another), 11 (requiring "a single ***unique*** supply signal"), 13 (requiring a "second voltage" "lower than" a "first voltage"). There is no such requirement in the asserted claims, underscoring that the two signals may or may not be the same.

There is no legal reason why the same element of an accused product cannot as a general

matter satisfy two distinct claim limitations. *See, e.g.*, *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231–32 (Fed. Cir. 2011) (affirming jury finding of literal infringement when the same features in the accused product satisfied two separately recited elements). [redacted]

Intel's conclusory argument that the specification "describes VDD and VSS as different voltage signals," Mot. at 9, is followed by a string of citations that, at most, only show separate discussion of both supply and reference signals (which are sometimes labeled "VDD" and "VSS"), but not any requirement that the elements must be embodied by distinct features in the accused product. *Compare*, *e.g.*, '922 Pat. at 5:63–67 (discussing "VDD" but not "VSS"), *with* Mot. at 9 (citing same). And while Intel cites Figures 1–6 as "depicting" VDD and VSS as distinct, *see* Mot. at 9, other parts of the specification ***not*** cited by Intel contemplate signals provided by multiple sources in some embodiments and by a common source in others, *see, e.g.*, '922 Pat. at 4:46–57 (embodiments where "supply signals" are generated by three sources or one source), 5:4–17 (stating that circuits may connect to "separate nodes of the same reference signal," "the same node of a single reference signal," and "two or more distinct reference sources"), and embodiments in which voltages that are depicted as distinct in one of the patent's figures are nevertheless the same. *See id.* at 4:49–55 (controls depicted as providing "different" supply signals in Figure 1 may in "other embodiments" provide signals "with the same or similar supply voltages"). *See, e.g.*, *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1338–39 (Fed. Cir. 2001) (reversing summary judgment of noninfringement due to an erroneous claim construction based on a patent's figures).

Intel relies on unexplained citations to 23 paragraphs of its own expert report in arguing that a POSA would understand that the accused products do not contain a "supply signal" or a "reference signal" as claimed, *see* Mot. at 9 (citing ECF 579-14 (Apsel Reb. Rpt.) ¶¶ 144–67), while largely disregarding VLSI's opposite expert evidence, *see, e.g.*, ECF 579-10 (Mangione-Smith Rpt.) ¶¶

196–203, 230–34 (identifying these signals); ECF 579-12 (Rep. Rpt.) ¶¶ 133–65 (responding to Intel's supply and reference signal arguments). [redacted] *id.* at 140:13–141:6. The experts' full testimony highlights the numerous factual disputes here. *See, e.g.*, *Cradle IP, LLC v. Tex. Instruments, Inc.*, 5 F. Supp. 3d 626, 650 (D. Del. 2013) (denying summary judgment when experts disagreed about a term's plain meaning), *aff'd*, 588 F. App'x 1000 (Fed. Cir. 2015).

Second, while Intel argues that the parenthetical "VSS" in asserted claim 4 is "limiting," Intel does not offer any evidence that a limiting "VSS" would exclude the accused "reference signal" or explain what it contends the term would mean. The patent's discussion of embodiments of Figure 3—which Intel identifies as purportedly disclosing "[t]he stated purpose of the reference power converter"—does not answer the latter question at all, let alone in a way that excludes the accused "reference signal." Mot. at 10. If Intel is repeating its argument that a "supply signal" and "reference signal" cannot provide the same voltage, this is incorrect, as explained above. VLSI does not agree that VSS "has no meaning . . . because it appears in parentheses" in claim 4. *Id.* The parenthetical in "reference signal (VSS)" refers to examples of the "reference signal" that are labeled "VSS" in the specification and figures, without incorporating every feature of these examples into the

claims—a practice acknowledged both by courts, *see, e.g.*, *NXP USA, Inc. v. Impinj, Inc.*, 2022 WL 16716226, at *8–10 (W.D. Wash. Nov. 4, 2022) (parenthetical in "specific useful data (nxUDB)" not limiting); *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 2015 WL 6956722, at *5–7 (E.D. Tex. Nov. 9, 2015) (parentheticals in multiple terms not limiting), *Hochstein v. Microsoft Corp.*, 2009 WL 1838975, at *12–16 (E.D. Mich. June 22, 2009) (parenthetical in "communication couplers (L1, L2)" not limiting), and by the then-operative patent regulations, which state that the use of such "reference characters" was "considered as having no effect on the scope of the claims." MPEP § 608.01(m). Intel's only citation on this point is inapposite; the "25–30 mesh" parenthetical in *Janssen Pharmaceutica, N.V. v. Eon Labs Manufacturing, Inc.*, 124 F. App'x 425 (Fed. Cir. 2005), did not label a claim element (as "VSS" labels exemplary "reference signals" in the '922 specification); it provided numerical reference to an "industry standard sieving process" for specifying the particular size of a claim element (as "0.0 volts" might specify a particular voltage of a "reference signal"), *id.* at 428.

[redacted] ECF 579-10 ¶¶ 249–57; ECF 579-12 ¶¶ 160–62.

Intel's motion, at most, raises contested factual issues about whether the accused products contain a "reference signal" and "supply signal." The motion should be denied.

IV. THE '922 PATENT IS NOT INDEFINITE

Intel's indefiniteness arguments fail for multiple reasons. First, the preamble term "power island" is not a limitation in the asserted claims. Second, even if the term had been a limitation, Intel's motion at most identifies a dispute about how a person of ordinary skill in the art would understand the term—a highly factual dispute for which Intel offers only attorney argument.

Intel, strikingly, does not argue that "power island" is limiting here. Preamble language is not limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Acceleration Bay, LLC v. Activision Blizzard Inc.*, 908 F.3d 765, 770 (Fed. Cir. 2018) (quoting *Catalina Mktg. Int'l, Inc. v.*

Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002)). Absent a specific reason to find it limiting, it is not. *See Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1347 (Fed. Cir. 2012) ("[A]s a general rule[,] preamble language is not treated as limiting.").

The "power island" preamble language here is not limiting. Claims 4 and 5, which are representative for this purpose as Intel did not make indefiniteness arguments distinguishing among asserted claims, depend from claim 1. In claim 1, "power island" appears only in the preamble. As common sense in this context would suggest and as VLSI's expert confirms, a "power island" in the sense of claim 1 is simply a system having the components that are recited in the body of claim 1: a structurally complete invention. ECF 617-11 (Mangione-Smith Rep. Rpt.) ¶¶ 100–13; *Acceleration Bay*, 908 F.3d at 770–71 (preamble term not limiting when only in preamble). In claims 4 and 5, outside of the preambles ("the power island of claim 1, further comprising") there is only one appearance of the term "power island": in claim 4, where an earlier-recited "reference line" is referred to again using the phrase "the reference line of the power island." '922 Pat. at 9:53. In context, including that the only "reference line" recited anywhere in any claim of the '922 Patent is the "reference line" within claim 4, a "power island" is simply a system having the components recited in the body of the claim. *See IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1427, 1434 (Fed. Cir. 2000) (preamble's "control apparatus" was non-limiting name for structurally complete invention even when body referred to "said apparatus").

Intel attempts to distract from the operative claim language by selectively quoting the high-level "Background" section of the patent. But that section goes on to discuss features that in certain embodiments power islands may "typically have," aspects of how components of power islands "may be" operated, and drawbacks of "conventional" implementations of power islands. '922 Pat. at 1:33–37, 1:46–50; *see also* Mot. at 11:22–28 (discussing this language). This background material only confirms that the preamble's recitations of "power island" refer to an intended use of the invention. *See Acceleration Bay*, 908 F.3d at 770 (preamble reciting intended use was not limiting).

Intel's cases, addressing terms of degree, are inapposite because "power island" is not a term of degree. Intel's arguments also erroneously presume that the claim preambles incorporate aspects of the "Background" section as limitations. None of Intel's cases address preamble language.

To any extent that Intel now seeks to argue that the asserted claims' references to "different" or "partially different" power characteristics render them indefinite, such argument has been waived. Intel never previously disclosed this argument—not in Intel's 2018 pre-*Markman* identification of allegedly indefinite terms, ECF 106 at 2:4–6, during claim construction briefing, *see, e.g.*, ECF 118 (joint claim construction statement) at 2 n.2; ECF 241 (*Markman* order) at 5:3–9, in any version of Intel's invalidity contentions, *see, e.g.*, Ex. 11 (Jan. 26, 2022 Amended Invalidity Contentions) at 1377:8–21, and in expert reports (which Intel's motion does not cite), *see, e.g.*, Ex. 12 (Apsel Rpt.) ¶¶ 1180–84; ECF 579-14 (Apsel Reb. Rpt.) ¶¶ 152–53—although these materials all show that Intel intended to make section 112 arguments and was aware of its duty to disclose them. Arguments never disclosed under Patent Local Rule 3–3 are untimely and waived, *see, e.g.*, *Hewlett Packard Co. v. ServiceNow, Inc.*, 2016 WL 692828, at *4 (N.D. Cal. Feb. 19, 2016) (denying motion to amend invalidity contentions to add section 112 theory disclosed for the first time in *Markman* briefing); *Verinata Health, Inc. v. Sequenom, Inc.*, 2014 WL 4100638, at *3 (N.D. Cal. Aug. 20, 2014) (striking invalidity theory disclosed for the first time in expert reports), barring summary judgment in Intel's favor, *see, e.g.*, *Power Integrations, Inc. v. ON Semiconductor Corp.*, 396 F. Supp. 3d 851, 864 (N.D. Cal. 2019) (denying motion for summary judgment premised upon claim construction disclosed for the first time during summary judgment briefing).

[redacted] Viewed in context, the isolated excerpts cited by Intel do not even support its position. Moreover, inventor testimony has minimal probative value in any definiteness analysis. *Am. River Nutrition, LLC v. Beijing Gingko Grp. Biological Tech. Co.*, 419 F. Supp. 3d 1226, 1237 n.4 (C.D. Cal. 2020) (reversing judgment of indefiniteness premised upon inventor testimony (citing *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1380 (Fed. Cir. 2000))).

Tellingly, during inter partes review of the '922 Patent's claims, Intel did not argue that the

preambles were limiting, *Intel Corp. v. VLSI Tech. LLC*, No. IPR2018-01033, Paper No. 3 at 37, 51 (P.T.A.B. June 21, 2018), and both Intel and its expert seemed to understand the term "power island," *see, e.g.*, *id.* at 6 (arguing that "circuit designers long ago developed the concept of 'power islands'" and that the "concept of power islands has been known since . . . a decade ago"); *id.* at 33 (referring to the "specification's clear definition of 'power island'"). Even if Intel were permitted to change its position here, that would present at most a disputed question of fact. VLSI's expert has shown that the accused products contain "power islands" under the plain and ordinary meaning of the term, and Intel's belated arguments to the contrary cannot be summarily adjudicated. ECF 617-11 (Mangione-Smith Reply Rpt.) ¶¶ 171–78; *Cradle IP*, 5 F. Supp. 3d at 650 (no summary judgment when experts disagreed about term's plain and ordinary meaning).

V. INTEL INFRINGES THE '806 PATENT

Intel's motion focuses on the Court's construction of the term "when in a second mode of operation." Mot. at 13. The Court construed this term to have its "[p]lain and ordinary meaning, which includes the requirement of claim 11 that when in the second mode of operation the voltage(s) supplied to the first and second memory, respectively, must be lower than the minimum necessary for the first mode of operation." ECF 241 (*Markman* Order) at 6. The evidence shows infringement under precisely that construction. Though Intel may dispute VLSI's reasonable interpretation of the technical evidence, that is no basis to deny VLSI its right to a trial by jury.

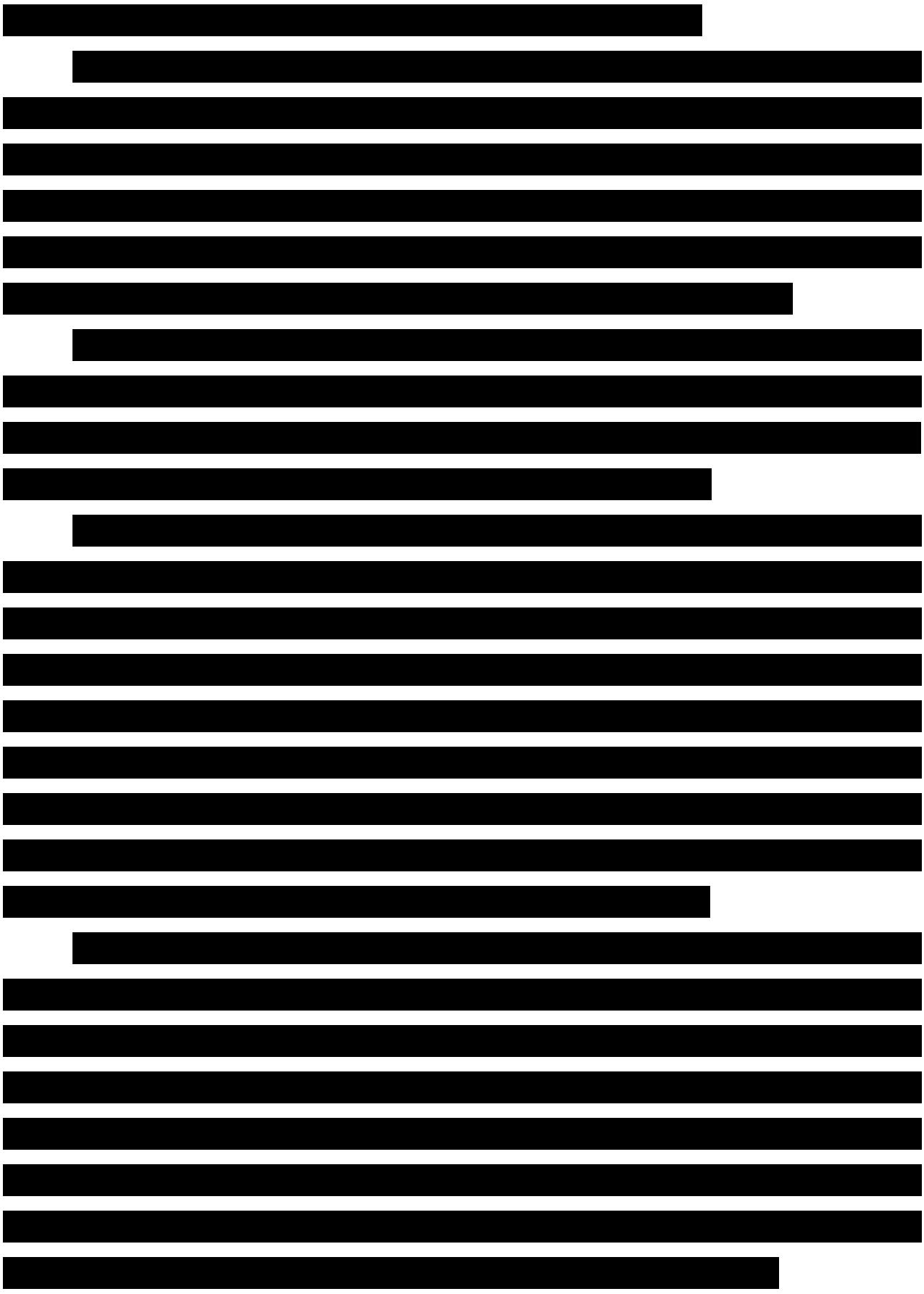
[redacted]

As an initial matter, for clarity, the "minimum operating voltage" at issue here is not intended to refer to "the first" or "the second" minimum operating voltage of claim 11. These minima are

properties of the memory ***cells*** (building blocks) of the memories, and Dr. Conte addresses these minimum operating voltages in his analysis. Ex. 1 (Conte Rpt.) ¶ 902–32, 750. The "minimum operating voltage" to which Intel's argument refers here is a property of the first ***memory***, and that term is not explicitly recited in claim 11. It is referenced in the Court's construction.

[redacted]

[1] The transcript mis-transcribes "is at," as used by the questioner and recorded on video, as "adds."



[redacted]

VI. INTEL INFRINGES THE '672 PATENT

A. Intel's "Current Process"

[redacted]

[redacted]

B. Intel's "Discontinued Process"

[redacted]

[redacted]

VII. INTEL'S LICENSE DEFENSE FAILS AS A MATTER OF LAW

Intel's summary judgment motion based on a 2012 settlement agreement with non-party

Finjan ("Finjan Settlement") fails for at least three independent reasons: (1) Intel's defense is barred by res judicata and collateral estoppel; (2) Intel cannot show that VLSI is bound by the Finjan Settlement; and (3) Intel cannot show that VLSI's patents are "Finjan's Patents." VLSI cross-moved for summary judgment on Intel's defense, and incorporates by reference its motion and supporting evidence. ECF 586 ("Cross Mot.") at 1–15; ECF 586-02–42 (Cross Mot. Exs. 1–41) ("[CM Ex.]").

First, as explained in VLSI's Cross-Motion, Intel's license defense is precluded by res judicata and collateral estoppel. *See* Cross Mot. at 4–6; *e.g.*, *Arrigo v. Link*, 836 F.3d 787, 799 (7th Cir. 2016). In a prior infringement action between the same parties, Intel asserted the exact same license defense it attempts to reassert here. That district court squarely ruled against Intel on the merits, *VLSI Tech. LLC v. Intel Corp.*, 2022 WL 1261322, at *2–4 (W.D. Tex. Apr. 21, 2022), and entered final judgment against Intel, [CM Ex. 17] (Final Judgment).

Intel argues that decisions in the alternative are not binding for purposes of collateral estoppel, citing *Comair Rotron, Inc. v. Nippon Densan Corp.*, 49 F.3d 1535 (Fed. Cir. 1995). There, the Federal Circuit held that a court's finding of non-infringement by a non-party in the context of damages was not essential to the ruling, and therefore the plaintiff was not barred from later suing that non-party for infringement. *Id.* at 1539. This case is nothing like *Comair*—here, in an action between these same parties, Judge Albright expressly found against Intel on the merits of the same license defense now asserted. Those findings (including that "VLSI is not bound by that license," *VLSI*, 2022 WL 1261322, at *3–4), were essential to Judge Albright's ruling on the license issue. Res judicata and collateral estoppel squarely bar Intel's license defense here. Cross Mot. at 6–7.

[redacted]

[redacted]

Intel's cases are inapposite. For example, in *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, the court found a non-compete binding on "affiliates" created by and "under the control of a party to the agreement," reasoning that holding otherwise would permit the contracting party to avoid its non-compete obligations. 213 A.3d 39, 57–58 & n.86 (Del. 2019). Likewise, in *MicroStrategy Inc. v. Acacia Rsch. Corp.*, an agreement bound a "wholly-owned subsidiary" of a named party. 2010 WL 5550455, at *12 (Del. Ch. Dec. 30, 2010). Here it is undisputed that Finjan was not involved in VLSI's creation, VLSI has never been "under the control of" Finjan, and VLSI's patents have nothing to do with Finjan. *E.g.*, [CM Ex. 13] at 96:21–97:8; [CM Ex. 2] at -646. Likewise inapposite is *Oyster Optics, LLC v. Infinera Corp.*, which held that a party (such as Finjan) may contract to benefit future affiliates of the opposing party (such as Intel). 843 F. App'x 298, 300–02 (Fed. Cir. 2021). But that holding is irrelevant here, since this case does not involve Finjan suing Intel or a new Intel affiliate. *See VLSI*, 2022 WL 1261322, at *3.

[redacted]

VIII. INTEL IS NOT ENTITLED TO SUMMARY JUDGMENT AS TO WILLFUL INFRINGEMENT, INDIRECT INFRINGEMENT, OR ENHANCED DAMAGES

Intel's motion regarding knowledge of infringement should be denied for multiple reasons. Indeed, a highly similar motion by Intel was already denied in other litigation between the parties.

See generally ECF 586-18 (Order, *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-CV-57 (W.D. Tex. Feb. 19, 2021). Intel's knowledge of its infringement has only grown since then.

A. Intel Had, Or Should Have Had, The Requisite Pre-Suit Knowledge

"[I]ndirect infringement requires knowledge of the underlying direct infringement." *Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1364 (Fed. Cir. 2016). Similarly, willful infringement requires "[t]he subjective willfulness of a patent infringer, intentional or knowing [but] without regard to whether his infringement was objectively reckless." *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93, 105 (2016); *see also Global-Tech Appliances, Inc. v. SEB S.A.*, 563 U.S. 754, 766 (2011) (willful blindness satisfies knowledge); *Liquid Dynamics Corp. v. Vaughan Co.*, 449 F.3d 1209, 1225 (Fed. Cir. 2006) (willful infringement requires "considering the totality of the circumstances"). The totality of circumstances here, viewed most favorably for VLSI, sufficiently supports a finding that, even pre-suit, Intel knew or should have known of its infringement.

[redacted]

Further, it is undisputed that Intel was aware of the '836 patent because it cited the patent's application during prosecution. Ex. 27 (File History) at 34, 42–57. This, too, supports a finding of the requisite knowledge. *See, e.g.*, *MasterObjects, Inc. v. Amazon.com, Inc.*, 2021 WL 4685306, at *4 (N.D. Cal. Oct. 7, 2021) (finding knowledge where patent cited in patent application).

[redacted]

[redacted] This willful blindness is a further part of "the panoply of conduct alleged by" VLSI. *Intel Corp. v. Future Link Sys., LLC*, 268 F. Supp. 3d 605, 623 (D. Del. 2017) (denying summary judgment because of Intel's willful blindness).

B. Intel Had Even Further Post-Suit Knowledge Of Each Asserted Patent

VLSI's claims for post-filing willfulness and indirect infringement are supported by still further evidence. VLSI served Intel with its complaint on October 16, 2017, ECF 1, 16, infringement contentions on January 18, 2018, and refinements to those contentions on three subsequent occasions, *see, e.g.* 402-17 (3d am.). Intel's assertion that indirect and willful infringement cannot be based on post-filing conduct alone is doubly wrong. Factually, these claims are based on a combination of pre- and post-filing facts as set forth above. And legally, these claims can be based on post-filing conduct alone. *See, e.g.*, *In re Bill of Lading Transmission & Processing Sys. Pat. Litig.*, 681 F.3d 1323, 1345 (Fed. Cir. 2012) (post-filing knowledge sufficient where "[defendant] became aware of the . . . patent . . . when it was served with the complaint"); *PersonalWeb Techs. LLC v. Int'l Bus. Machs. Corp.*, 2017 WL 2180980, at *20–21 (N.D. Cal. May 18, 2017) (allowing willfulness where defendant "continued its infringement since at least the filing of the complaint"); *Symantec Corp. v. Veeam Software Corp.*, 2012 WL 1965832, at *4–5 (N.D. Cal. May 31, 2012) (complaint creates knowledge). Even Intel's case, *Dali Wireless, Inc. v. Corning Optical Commc'ns, Inc.*, 638 F. Supp. 3d 1088, 1099 (N.D. Cal. 2022), makes clear that "a well-pled, detailed complaint laying out a clear case of infringement could supply the knowledge . . . required for willfulness."

Intel's contrary cases embrace reasoning that has been explicitly rejected by district courts and implicitly by the Federal Circuit. Both *Splunk Inc. v. Cribl, Inc.*, 2023 WL 2562875 (N.D. Cal. Mar. 17, 2023), and *Sonos, Inc. v. Google LLC*, 591 F. Supp. 3d 638 (N.D. Cal. 2022), premise their holdings on a policy rationale "encouraging the practice of pre-suit notice through a cease-and-desist letter . . . . in order to give the alleged infringer a meaningful opportunity to cease infringement or to get a license." *Sonos*, 591 F. Supp. 3d at 643; *see also ZapFraud, Inc. v. Barracuda Networks,*

Inc., 528 F. Supp. 3d 247, 250 (D. Del. 2021) (similar).

In addition, numerous courts have criticized Intel's arguments. *See, e.g.*, *CAP Co. v. McAfee, Inc.*, 2015 WL 3945875, at *5 (N.D. Cal. June 26, 2015) ("[T]he cure imposed . . . is worse than the purported disease . . . . [I]t would result in a pro forma notice letter from the patentee, followed by an immediate lawsuit in order to head off a declaratory judgment suit by the alleged infringer."); *Therabody, Inc. v. Tzumi Elecs. LLC*, 2022 WL 17826642, at *12 (S.D.N.Y. Dec. 19, 2022) (noting "little practical difference between a pre-complaint notice letter . . . and a . . . complaint"). Intel's policy rationale is inapplicable here, where the defendant has demonstrated unwavering unwillingness to cease infringement of NXP's former patents, which VLSI has already successfully tried to verdict against Intel twice. *See, e.g.*, ECF 586-18. Indeed, the Federal Circuit has rejected similarly formalistic requirements. *See Mentor Graphics Corp. v. EVE-USA, Inc.*, 851 F.3d 1275, 1296 (Fed. Cir. 2017) (district court erred in precluding patentee from presenting evidence of willful infringement because it relied exclusively on post-suit willfulness conduct, and "there is no rigid rule that a patentee must seek a preliminary injunction"). *Mentor Graphics* is all the more applicable here because the patents Intel was held to infringe share inventors with the patents in suit. *See, e.g.*, '806 Pat.; Ex. 30 ('373 Patent asserted in W.D. Tex.). And, Intel has even relied on the knowledge of infringement provided by the complaint to support its (ultimately dismissed) claims in another offensive case it filed, emphasizing to this very Court that "it is not possible to fully escape [VLSI's] assertions" or to design around them. Ex. 31 (*Intel v. Fortress*) ¶ 129.

C. Intel Had Even Further Post-Suit Knowledge Of Each Asserted Patent

Intel requests that the Court decide, prematurely, that VLSI is not entitled to enhanced damages. There is no reason for such a departure from normal practice. If the jury finds Intel willfully infringed, the Court should evaluate enhanced damages in a fully informed manner. *See, e.g.*, *Jurgens v. CBK, Ltd.*, 80 F.3d 1566, 1570 (Fed. Cir. 1996) ("First, the fact-finder must determine whether an infringer is guilty of conduct upon which increased damages may be based. If so, the court then determines . . . whether . . . to increase the damages award . . . .").

IX. CONCLUSION

VLSI requests that the Court deny Intel's Motion for Summary Judgment in its entirety.

Dated: September 21, 2023

Respectfully submitted,

By: */s/ Charlotte J. Wen*

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document has been served via electronic mail on September 21, 2023 on counsel of record for Intel Corp. I certify under penalty of perjury and the laws of the United States that the foregoing is true and correct.

Dated: September 21, 2023

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